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Tuning band alignment by CdS layers using a SILAR method to enhance TiO_2/CdS/CdSe quantum-dot solar-cell performance†

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We report tuning band alignment by optimized CdS layers using a SILAR method to achieve the recorded best performance with about 6% PCE in TiO_2/CdS/CdSe QDSSCs. Combining experimental and theoretical studies, we find that a better lattices match between CdS and TiO_2 assists the growth of CdSe, and the combined effect of charge transfer and surface dipole moment at the TiO_2/CdS/CdSe interface shifts the energy levels of TiO_2 upward and increases V_{oc} of the solar cells. More importantly, the band gap of CdS buffer layers is sensitive to the distortion induced by lattice mismatch and numbers of CdS layers. For example, the barrier for charge transfer disappears when there are more than 4 layers of CdS, facilitating the charge injection from CdSe to TiO_2.

As an alternative renewable energy source, different kinds of solar cells have been developed in the past decades.[1] To improve the efficiency of cells, the design and optimization of an interface have played an important role, since photoelectron separation is closely associated with the kinetics of the electron-transfer processes at the interface.[2,3] As for the quantum-dot sensitized solar cells (QDSSCs), which have recently attracted much interest as promising photoelectric conversion devices due to their tunable adsorption band, high absorption coefficient and multiple exciton effect,[4] an important interface engineering process is used to insert a CdS buffer layer between TiO_2 and CdSe in the CdSe sensitized anatase-TiO_2 system (TiO_2/CdS/CdSe) to enhance the efficiency of cells. It is generally believed that the presence of a CdS buffer layer on one hand promotes the growth of CdSe, and on the other hand facilitates electron injection from CdSe to TiO_2 by the reorganization of band levels between CdS and CdSe, that is, from type I to type II,[5–7] in which by definition, both the conduction band edge (E_{cb}) and valence band edge (E_{vb}) of CdSe are located in the band gap of TiO_2 in the type I structure, and both E_{cb} and E_{vb} of CdSe are higher than those of TiO_2 in the type II structure. Nevertheless, the role of CdS buffer layers is still under debate in other experiments. Some suggested that CdS buffer layers actually impede the injection of electrons from CdSe to TiO_2 due to the type-I energy alignment of CdS/CdSe and accelerate charge recombination at the TiO_2/sensitizer interface.[8] The others proposed that the CdS/CdSe quantum dots have a quasi-type-II band alignment with E_{cb} of CdS close to that of CdSe.[9,10] Hence, it is highly desirable to further clarify and get a deep understanding of the role that the CdS buffer layer plays in TiO_2/CdS/CdSe cells.

In addition, the optimization of the thickness of the CdS buffer layer is also investigated experimentally. Palomares *et al.*[11] reported the best cell efficiency for the CdS/CdSe co-sensitized TiO_2 system consisting of 6 cycles of CdS and 8 cycles of CdSe. While Lee *et al.*[12] found that 3 cycles of CdS plus 4 cycles of CdSe exhibits the best efficiency. Dai *et al.*[13] found that the increase of CdS cycles enhances the short circuit current density. All these experimental findings implied that optimizing the CdS buffer layer is vital for performances of TiO_2/CdS/CdSe cells, but the detailed mechanism is still unclear: what is the relationship between the thickness of the CdS buffer layer and the energy level alignment at the TiO_2/CdS/CdSe interface? How is the electronic structure of the CdS buffer layer tuned by the thickness (successive ionic layer adsorption and reaction (SILAR) cycles), especially within a two-side confined interface? Such deep insights would not only be helpful for the future interface design to improve the photovoltaic performance but also be of fundamental interest for science.

Herein, we constructed the TiO_2/CdS/CdSe cells with a CdS buffer layer deposited on TiO_2 through the SILAR method,[14] and tested their photovoltaic performance by varying the CdS buffer layer by controlling the SILAR cycles. Fig. 1a and b show a schematic diagram of the preparation process of TiO_2/CdS/CdSe QDSSCs and a schematic construction of each material and related interfaces of TiO_2/CdS/CdSe, respectively. For comparison, we also tried to prepare TiO_2/CdSe by using the chemical bath

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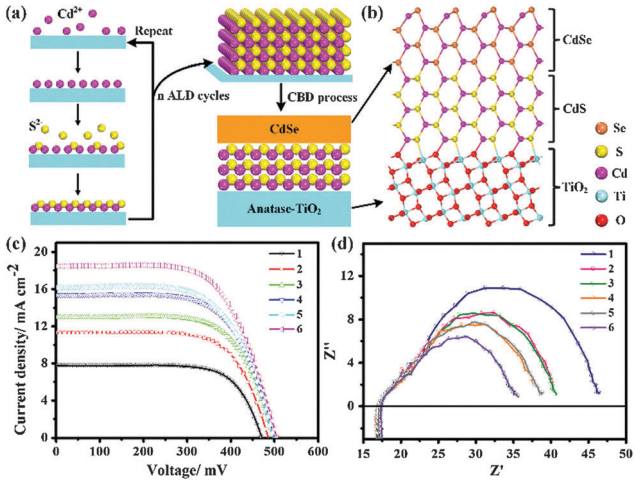

Fig. 1 (a) Schematic of the formation of a CdS buffer layer on the mesoporous anatase-TiO_2 film *via* the SILAR process. (b) Schematic construction of the TiO_2/CdS/CdSe configuration. (c) and (d) *J–V* characteristics and EIS spectra of TiO_2/(CdS)*n*/CdSe solar cells at different numbers of CdS cycles (*n*) measured in light under zero V bias, respectively. The number after labels denotes the cycles of CdS buffer layer deposition.

deposition (CBD) method and found that CdSe hardly grows on the TiO_2 film. Then, the thickness optimization of the TiO_2 film and CdSe was evaluated and the details are depicted in Section 1 of the ESI†. Using the optimized thickness of the TiO_2 film and CdSe, we further prepared the TiO_2/CdS/CdSe quantum-dot cells. The *J–V* characteristics of TiO_2/(CdS)*n*/CdSe cells (Fig. 1c and Tables S1, S3, ESI†) show that the current (J_{sc}) and power conversion efficiency (PCE%) increase more than double with the number of CdS cycles. For example, J_{sc} is increased from 7.77 to 18.47 mA cm^{-2}, while PCE is increased from 2.6% to 5.94% *vs.* n = 1 to 6 layers of CdS. In contrast, the open circuit voltage (V_{oc}) increases from 465 mV to 505 mV and the fill factor (FF) decreases from 0.72 to 0.64 *vs.* n = 1 to 6 layers of CdS, respectively, which means that both V_{oc} and FF change much less significantly *vs.* CdS layers. A higher V_{oc} suggests that E_{cb} of TiO_2 shifts upward with the increasing number of CdS cycles. A lower FF is probably because of the low driving force for the electron injection with the cycles of CdS. E_{cb} of CdS shifts downward with the increasing number of CdS cycles. The higher PCE of TiO_2/(CdS)6/CdSe is attributed to its broader light adsorption range which leads to a higher J_{sc} compared with that of TiO_2/(CdS)1/CdSe. In addition, PCE and all related factors (J_{sc}, V_{oc}, FF) almost remain constant after more than 6 layers of CdS (see Table S4, ESI†). The best performing device has an efficiency of about 6% (5.9–6.3% in different experiments), which is higher than those of other CdS/CdSe sensitized solar cells prepared in the same way[15–18] and is similar to the latest report (6.01%) in which CdS/CdSe are co-sensitized on TiO_2 nanowire-coated hollow spheres.[19] The electrochemical impedance spectroscopy (EIS) measurements of the cells (Fig. 1d) show that the conductivity of TiO_2/(CdS)*n*/CdSe cells is increased by the CdS cycles. The above observations implied that CdS layers with increasing cycles may broaden light adsorption and reduce the energy barrier for excited electron injection from the CdSe layer to TiO_2.

In addition, *J–V* curves also suggest that the voltage first increases with increasing CdS cycles and then comes to a saturation after 3 cycles of the CdS layer (Fig. 1c), indicating that the band levels of the CdS layer can be tuned by its cycles from higher to lower levels. So the following questions arise: (i) From the point of quantum-dot crystal growth, how the insertion of the CdS buffer layer promotes the growth of CdSe. (ii) From the point of tuning of the electronic structure, how the insertion of CdS layers with TiO_2/(CdS)*n*/CdSe quantum-dots affects their energy levels, and how does the number of CdS buffer layers by controlling SILAR cycles affect the band gap and alignment? To answer these questions, we did a comprehensive study on the TiO_2/CdS/CdSe interfacial properties using the DFT method in the following part.

The most important step is to establish a reasonable interface structure between anatase-TiO_2 and CdS for studying the TiO_2/CdS/CdSe composites. As depicted in Fig. 1a, for the CdS layer grown by SILAR on anatase-TiO_2, the TiO_2/CdS/CdSe samples were investigated by means of TEM analyses (Fig. S6, ESI†). We found that the (101) plane of TiO_2 and the (110) plane of CdSe are the most exposed surfaces, respectively, which are consistent with previous studies.[20,21] Therefore, the (101) surface of TiO_2 is chosen as the substrate. Based on the (2 × 2) supercell parameters of TiO_2(101) (10.87 × 7.73 $Å^2$), we found the nonpolar (110) face of cubic CdS, a (2 × 2) supercell (11.65 × 8.24 $Å^2$) to match best with the TiO_2(101) surface (the lattice mismatch less than 7%). Thus, the (110) surface of cubic CdS and CdSe is chosen as the contact surface according to the best lattice matching at the interface. While the mismatch between CdSe(110) (12.11 × 8.56 $Å^2$) and TiO_2(101) is beyond 11%, suggesting that the growth of CdSe on TiO_2 is difficult. The current results are consistent with experimental observations which suggests that CdS grows on the TiO_2 film more easily.[8] Fig. 1b and Fig. S1a and b (ESI†) show the interface bonded with the chemical bond (O–Cd) between the O atom of TiO_2 and the Cd atom of CdS in the optimized structures of TiO_2/CdS/CdSe and TiO_2/CdS, respectively. After relaxation, the average bond distance O–Cd is 2.38 Å, which is close to that of bulk Cd–O (2.34 Å), indicating a strong interaction between CdS and TiO_2 surfaces.

In the second step, we examined the geometric and electronic structures of TiO_2/(CdS)*n* and TiO_2/(CdS)*n*/CdSe by selecting 5 layers of CdS as a typical model as below. Fig. 2a shows the total or project density of states (TDOS or PDOS) of the TiO_2/(CdS)5 system, and the charge distributions of the states in the band edges are shown in Fig. 2a. It can be found that E_{vb} of CdS is lower than that of TiO_2 and E_{cb} of CdS is higher than that of TiO_2, indicating that the band alignment of the TiO_2/CdS system belongs to the type-II structure with both E_{vb} and E_{cb} of CdS located higher in the energy level than those of TiO_2. As a result, the electrons generated in CdS are energetically favorable to be transferred into TiO_2 and holes are transferred into CdS. From charge distribution, it is clear that little charge is localized at the O–Cd bonding interface, implying that charge recombination at the interface seems to be unfavorable. The band edge states are delocalized in bulk TiO_2 and bulk CdS, which is consistent with the prediction of the DOS results.

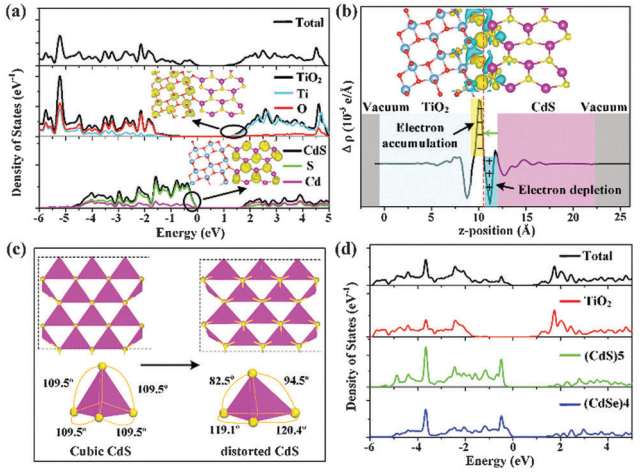

Fig. 2 (a) TDOS and PDOS of TiO_2/(CdS)5. The inset shows the charge states in the energy range of 0.00–0.50 eV below E_{vb} and above E_{cb} of TiO_2/CdS. (b) Charge density differences at the heterojunction and the corresponding planar average of the induced charge density difference for TiO_2/CdS. The yellow (cyan) region represents charge accumulation (depletion). (c) Distortion of the CdS layer from the cubic structure of the bulk structure to the distorted tetrahedral structure near the heterojunction interface. (d) TDOS and PDOS of TiO_2/CdS/CdSe composites.

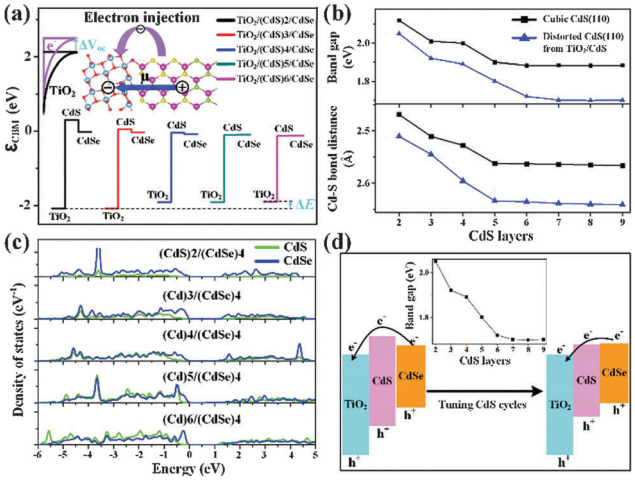

Fig. 3 (a) The E_{cb} energy of TiO_2, CdS, and CdSe with respect to their core potential energy in TiO_2/(CdS)n/CdSe. The inset shows the schematic of the dipole effect. (b) Energy gap of cubic and distorted CdS(110) surfaces as a function of CdS cycles. (c) PDOS of TiO_2/(CdS)n/(CdSe)4 with different CdS cycles. (d) Schematic of band alignment of TiO_2/(CdS)n/CdSe by tuning layers (n).

In addition, there is no interfacial gap state, and charges could be readily transferred across the interface under visible-light irradiation. Fig. 2b shows the three-dimensional charge density divergence by subtracting the electronic charge of a TiO_2/CdS composite from those of the CdS and TiO_2 structures and the charge redistribution along the z-direction normal to the interface. The planar-averaged charge density divergence along the z direction also exhibits charge redistribution. The positive (negative) values represent electron accumulation (depletion). It was found that the electrons are transferred from CdS to TiO_2, and more specifically, the electrons are transferred from Cd atoms to O atoms. Therefore, an interface dipole was generated in a direction from the CdS side to the TiO_2 side. After further checking the structural properties of TiO_2/CdS, it was found that, after relaxation, TiO_2 retains the bulk TiO_2-like structure but CdS induces a structural distortion. As depicted in Fig. 2c, the lattice mismatch at the interface leads to a change in the CdS structure from the cubic to a distorted tetrahedron. Compared with the cubic CdS, the average bond distance of Cd–S in the tetrahedron is lengthened from 2.562 Å to 2.635 Å, and such stress may affect its electronic structure. Besides, the DOS and PDOS of TiO_2/(CdS)5/CdSe are also calculated as shown in Fig. 2d, in which CdSe grains are constructed through isomorphic replacement of the surface S atoms by Se atoms in reconstructed four Cd–S layers since CdS/CdSe is a homojunction. The energy levels of TiO_2/CdS and CdS/CdSe suggested in Fig. 2d exhibit a type-II and a quasi-type-II structure, respectively. In the quasi-type-II structure of CdS/CdSe, E_{cb} of CdS is close to that of CdSe but E_{vb} of CdS is lower than that of CdSe. Therefore, the energy levels obtained by insertion of CdS layers may not impede the charge transfer, just as the experimental observation and previous experimental reports indicate.[5,6] Furthermore, the calculated electrostatic potential of the interface, deducing the electron transport route based on the electrostatic potential difference shown in Fig. S8 (ESI†), also agrees well with the DOS analysis.

Hence, the energy levels of TiO_2, CdS, and CdSe are assessed by aligning the E_{cb} energy with respect to their core potential energy, respectively. First, on one hand, as mentioned in Fig. 2b, the charge transfer from CdS to TiO_2 generates a dipole field at the heterojunction interface (inset of Fig. 3a), which leads to a downward shift of the conduction band of TiO_2. Such interface dipoles inducing energy level shifts have also been reported in other solar-cell systems.[22,23] On the other hand, the accumulation of electrons in TiO_2 shifts the conduction band of TiO_2 upward.[24–27] Thus, the shift of the TiO_2 conduction band is determined by the combined effect of charge transfer and surface dipole moment. To shed light on this issue, E_{cb} of TiO_2/(CdS)n/CdSe (n = 2–6) is shown in Fig. 3a. It was found that E_{cb} of TiO_2 increases with the increasing thickness of the CdS layer, because the dipole potential diminishes. The increased extent of $E_{cb}(TiO_2)$ is labeled as ΔE as shown in Fig. 3a. The increase of $E_{cb}(TiO_2)$ is beneficial to V_{oc} of the cell. Fig. 3a also suggests that the E_{cb} difference between CdS and TiO_2 reduces with the increasing CdS cycles, which would reduce the driving force for the electron injection. These results agree with the experimental observation as shown in Fig. 1c and Table S1 (ESI†). Second, band gaps can be tuned by the number of CdS layers in both ideal cubic CdS (from the ideal CdS crystal structure) with vacuum as the interface and the distorted tetrahedral CdS structure near the heterojunction interface shown in Fig. 2c and 3b, in which all band gaps first decrease rapidly with increasing CdS layers, and then to a nearly invariable value after 5–6 layers. This is because as the layers increase, the outer layers of CdS would suffer less stress from the interface and possess a more relaxed state. The enlarged Cd–S bonds suggest

a weaker interaction between Cd and S atoms with the increasing cycles, which would make electrons become more delocalized and itinerant, thus narrowing the band gap. Similar results are also found at the TiO_2/PbS interface, it was shown that the TiO_2 surface structure induces PbS bond angle distortions which changed the energy gap of the PbS QDs at the interface.[28] Thus, the band gap reduction (*vs.* n = 1 to 6 layer) affects the light adsorption range, resulting in high PCE and J_{sc}, as shown in Fig. 1c and Table S1 (ESI†). And above 6 layers, the band gap is invariantly consistent with the small change in photovoltaic parameters as shown in Table S4 (ESI†).

Therefore, the transition of energy levels from TiO_2 to CdSe can be tuned by the interface dipole and the band gap of CdS buffer, which can be controlled by SILAR cycles. Insight into the CdS layers *vs.* band energy levels of TiO_2/CdS/CdSe was further examined by analyzing the PDOS of TiO_2/(CdS)n/CdSe with different CdS layers, as shown in Fig. 3c, which shows that the CdS buffer layer serves as a barrier for charge transfer when the layers are under 4. Interestingly, the barrier disappears when the layers are 4 (n = 4) and more than 4 ($n > 4$), which would lead to facilitation of the charge injection from CdSe to TiO_2. Therefore, tuning CdS buffer layers by SILAR cycles to optimize the energy levels of TiO_2/CdS/CdSe quantum-dots can tune the band alignment to enhance the solar-cell performance as shown in Fig. 3d.

In summary, the role played by CdS buffer layers in TiO_2/CdS/CdSe was investigated based on experiments and theoretical calculations. The combined effect of charge transfer and dipole moment at the TiO_2/CdS/CdSe heterojunction interface produces an upward energy level shift for TiO_2. Besides, charges could be readily transferred across the interface under visible-light irradiation due to the absence of interfacial gap states. Most important of all, the band gap of the CdS buffer layer can be tuned by varying its number of layers, which were controllably formed by the SILAR process. Electrons could not be efficiently transferred when the CdS buffer layer was too thin (*e.g.* less than 4 layers of CdS), and tuning the layers of CdS can induce a suitable energy level alignment between CdS and CdSe (*e.g.* thicker than 4 layers of CdS). As a result, the reorganization of energy levels with the band alignment between TiO_2 and CdSe by insertion of an optimized CdS buffer layer forms a stepwise structure of band-edge levels to benefit photoelectron separation to enhance solar-cell performance. These findings provide insights into the design of high performance solar-cells with optimized buffer layers.

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